FIG. 1

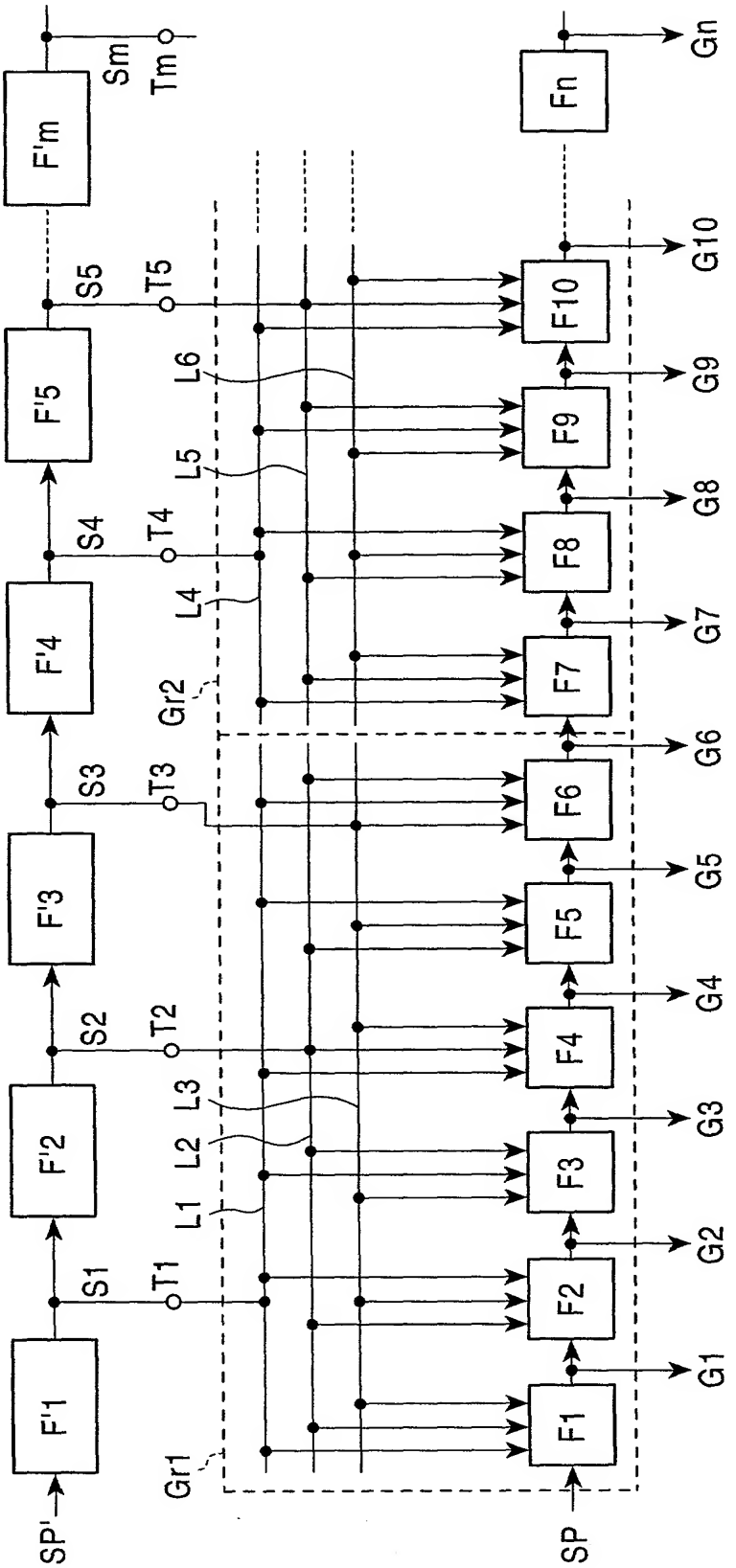
SP'
F'1
F'2
F'3
F'4
F'5
F'm
S1
S2
S3
S4
S5
Sm
T1
T2
T3
T4
T5
Tm
L1
L2
L3
L4
L5
L6
Gr1
Gr2
SP
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
Fn
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
Gn

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FIG. 2

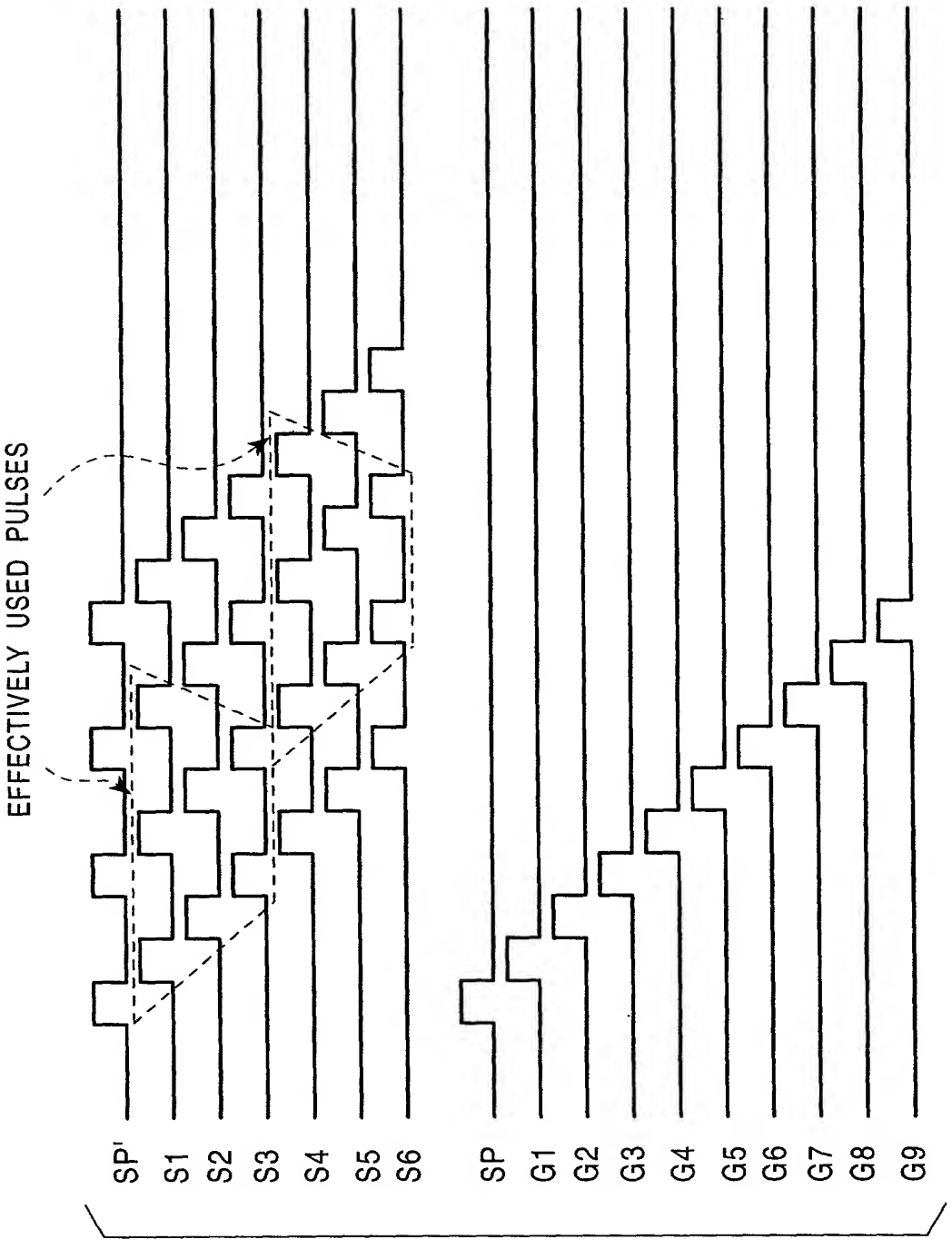

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FIG. 3

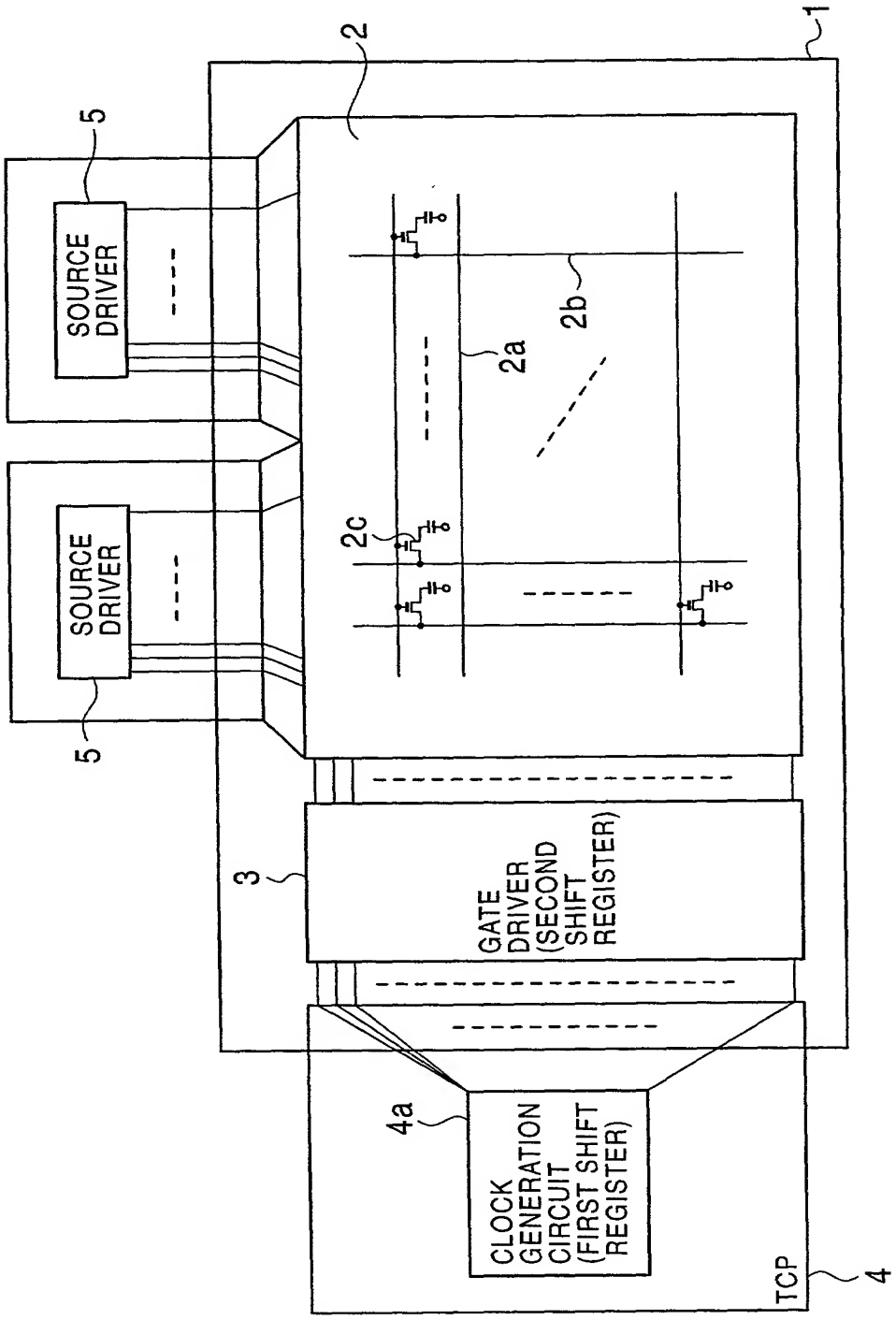


FIG. 4

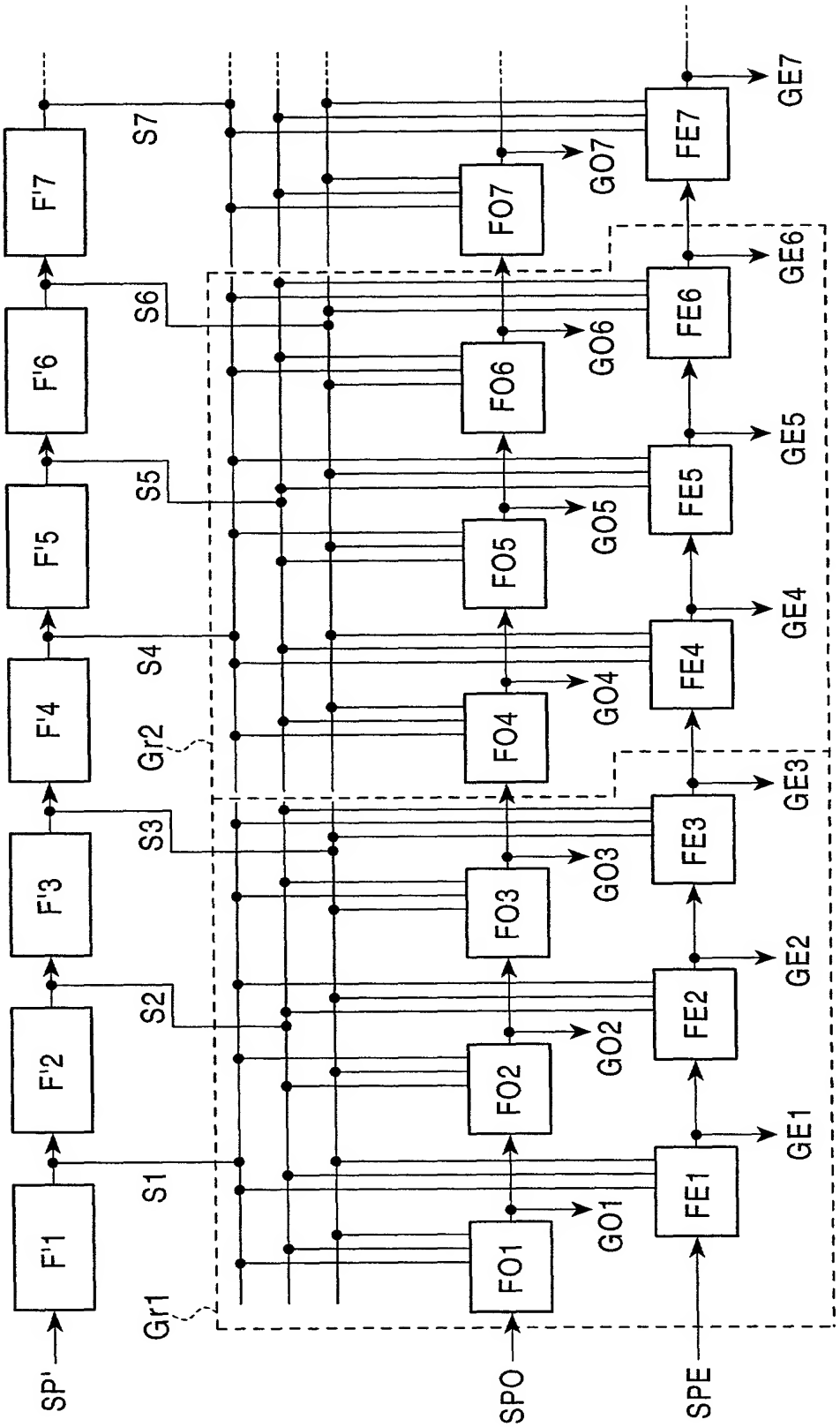

SP'
SPO
SPE
F'1
F'2
F'3
F'4
F'5
F'6
F'7
S1
S2
S3
S4
S5
S6
S7
Gr1
Gr2
FO1
FO2
FO3
FO4
FO5
FO6
FO7
GO1
GO2
GO3
GO4
GO5
GO6
GO7
FE1
FE2
FE3
FE4
FE5
FE6
FE7
GE1
GE2
GE3
GE4
GE5
GE6
GE7

FIG. 5

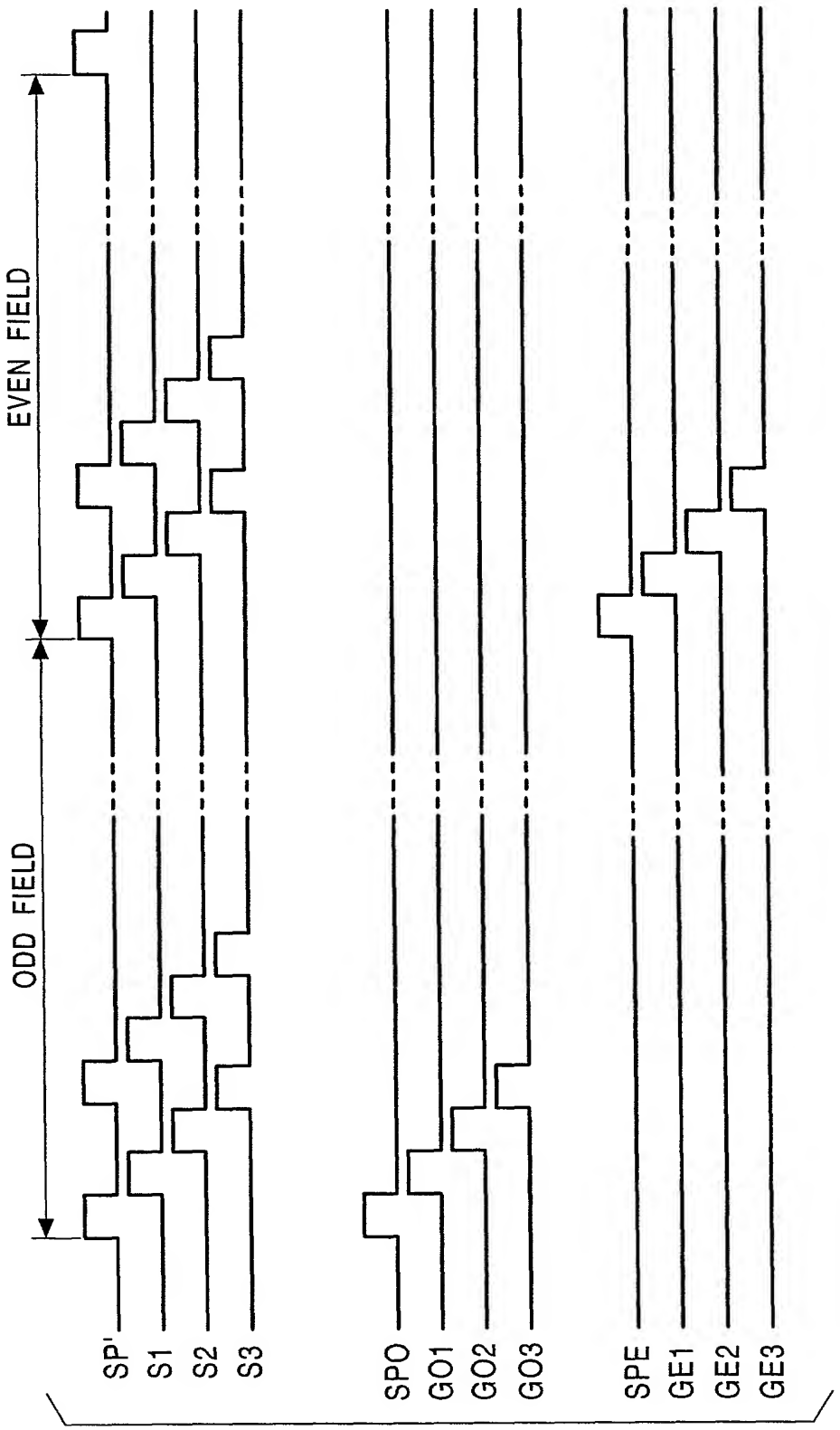


FIG. 6

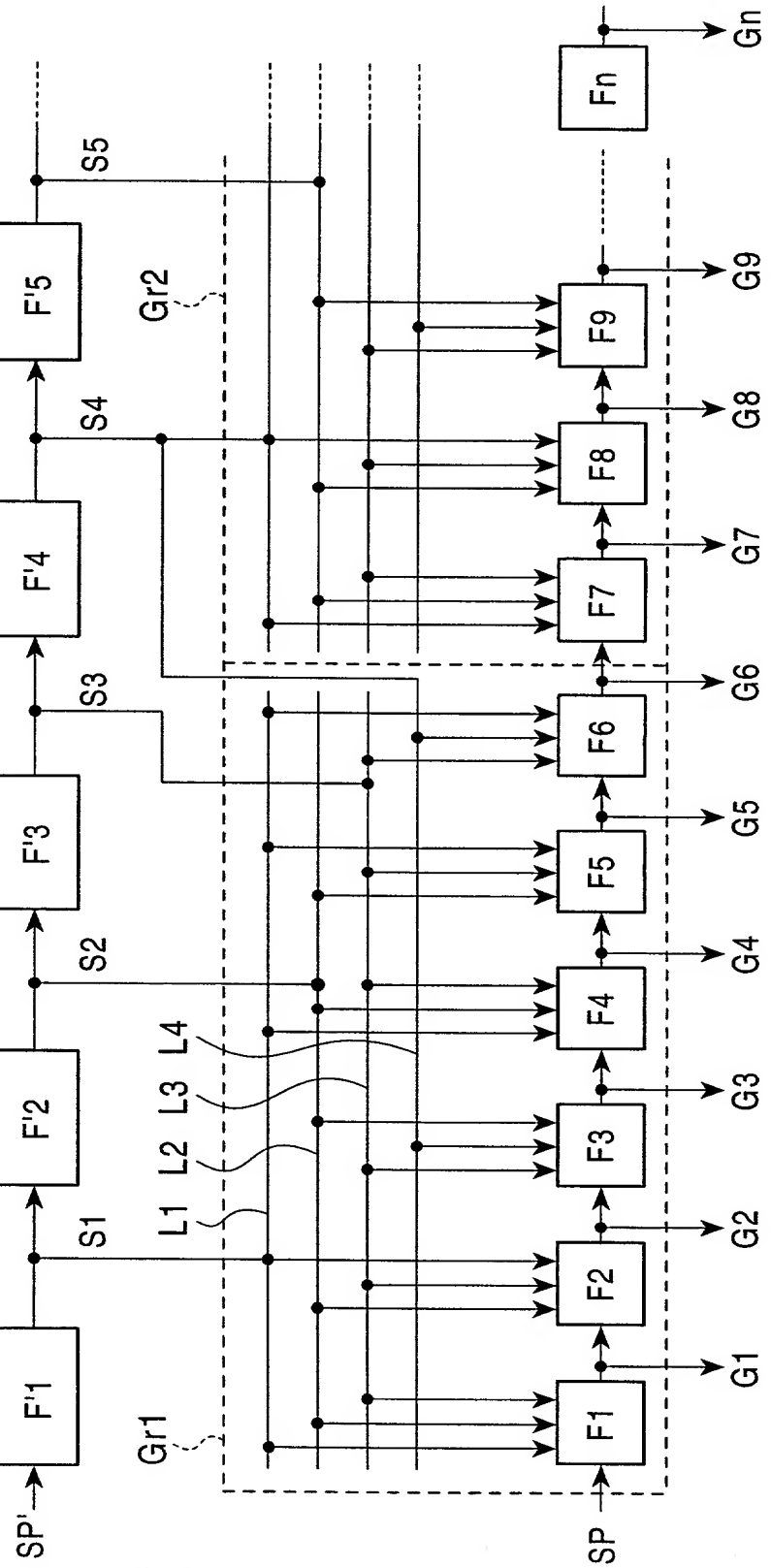

SP'
F'1
F'2
F'3
F'4
F'5
S1
S2
S3
S4
S5
Gr1
Gr2
L1
L2
L3
L4
SP
F1
F2
F3
F4
F5
F6
F7
F8
F9
Fn
G1
G2
G3
G4
G5
G6
G7
G8
G9
Gn

FIG. 7

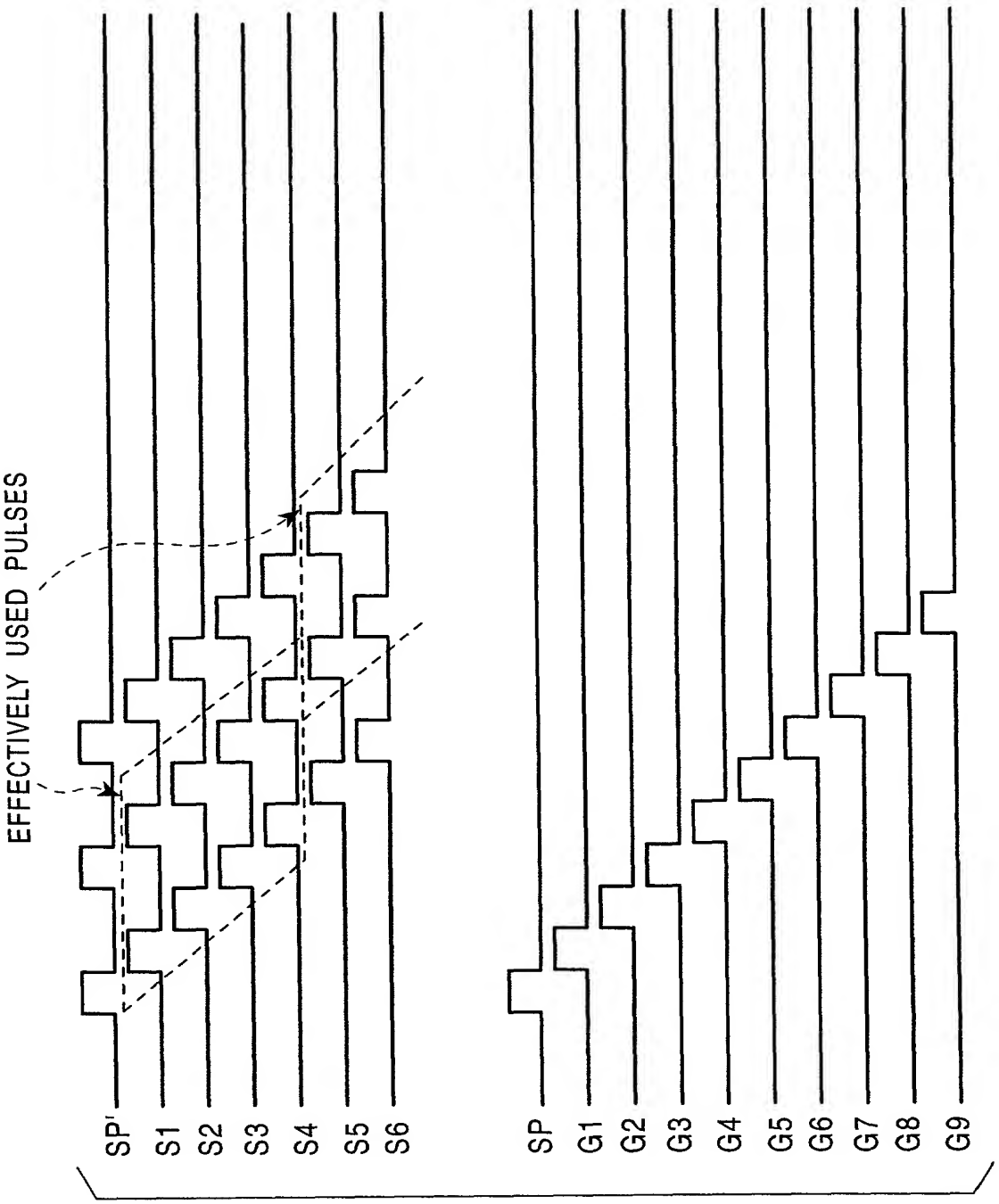

EFFECTIVELY USED PULSES
SP'
S1
S2
S3
S4
S5
S6
SP
G1
G2
G3
G4
G5
G6
G7
G8
G9

FIG. 8

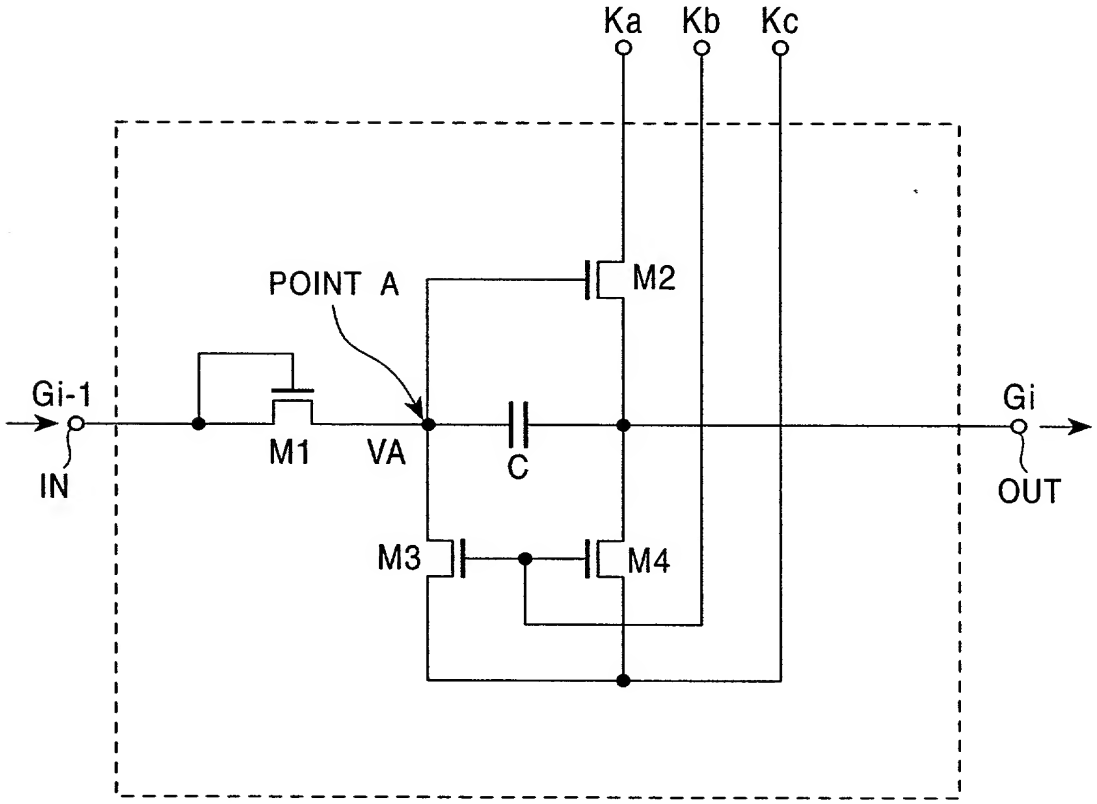


FIG. 9

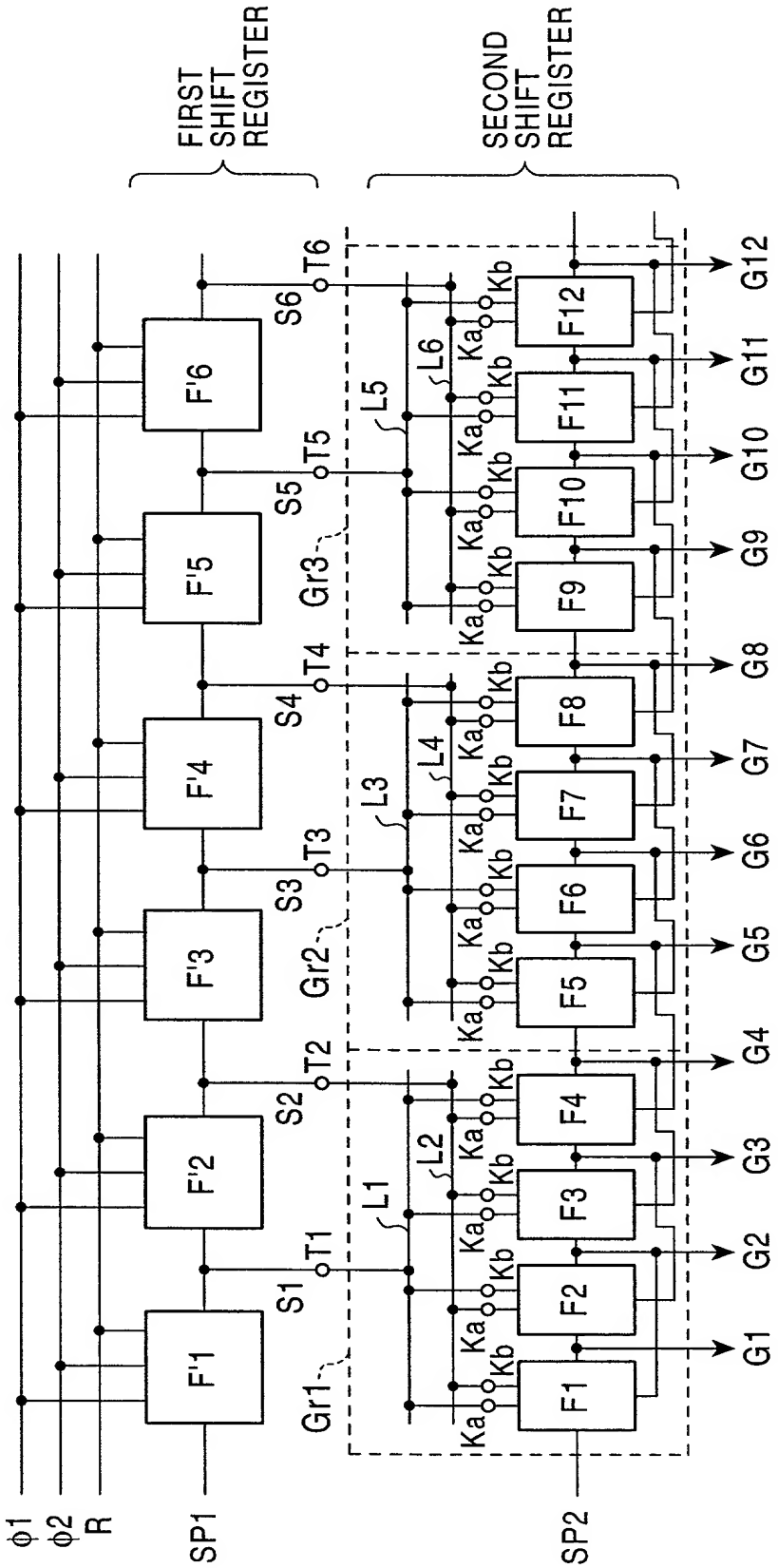

FIRST SHIFT REGISTER
SECOND SHIFT REGISTER
φ1
φ2
R
SP1
SP2
F'1
F'2
F'3
F'4
F'5
F'6
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
S1
S2
S3
S4
S5
S6
T1
T2
T3
T4
T5
T6
L1
L2
L3
L4
L5
L6
Gr1
Gr2
Gr3
Ka
Kb
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
G11
G12

FIG. 10

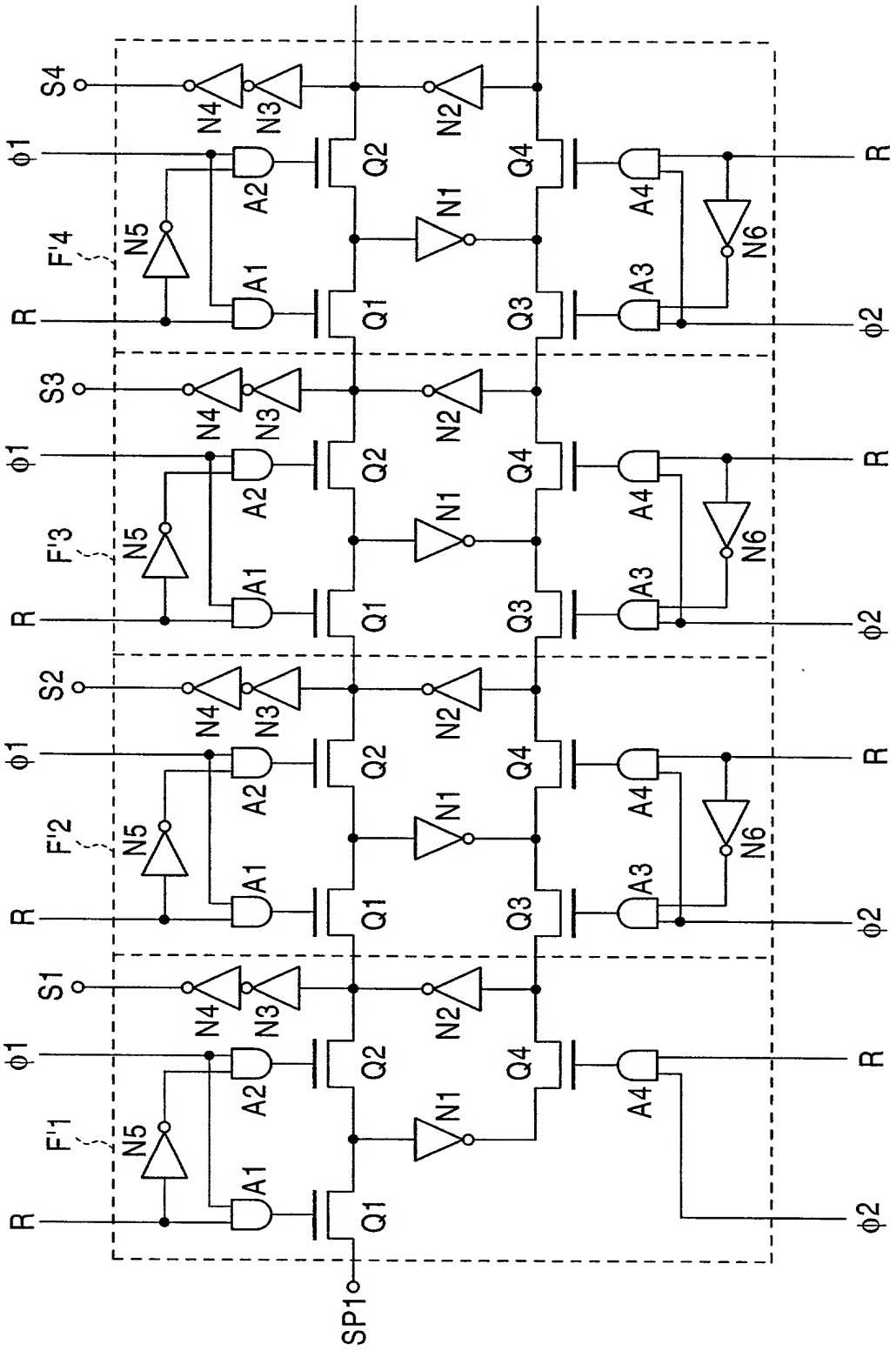

S4
S3
S2
S1
SP1
φ1
φ2
R
F'4
F'3
F'2
F'1
N1
N2
N3
N4
N5
N6
Q1
Q2
Q3
Q4
A1
A2
A3
A4

FIG. 11

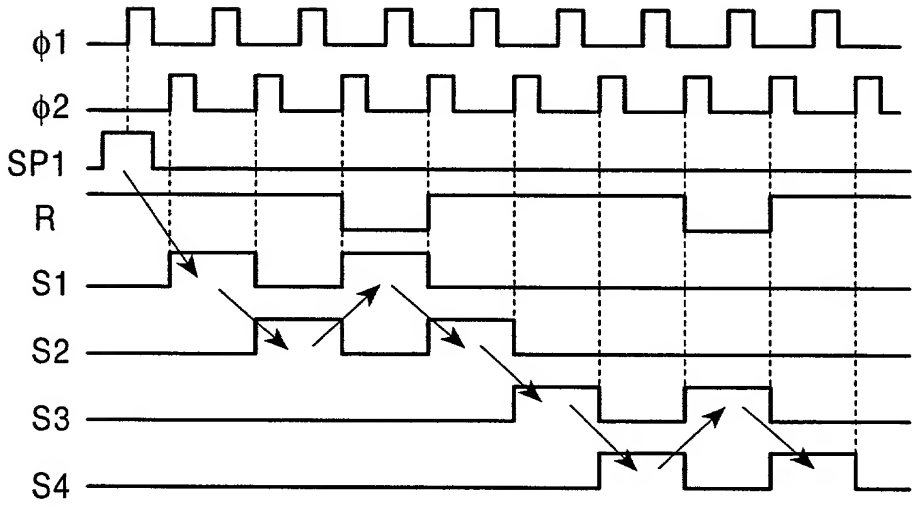


FIG. 12

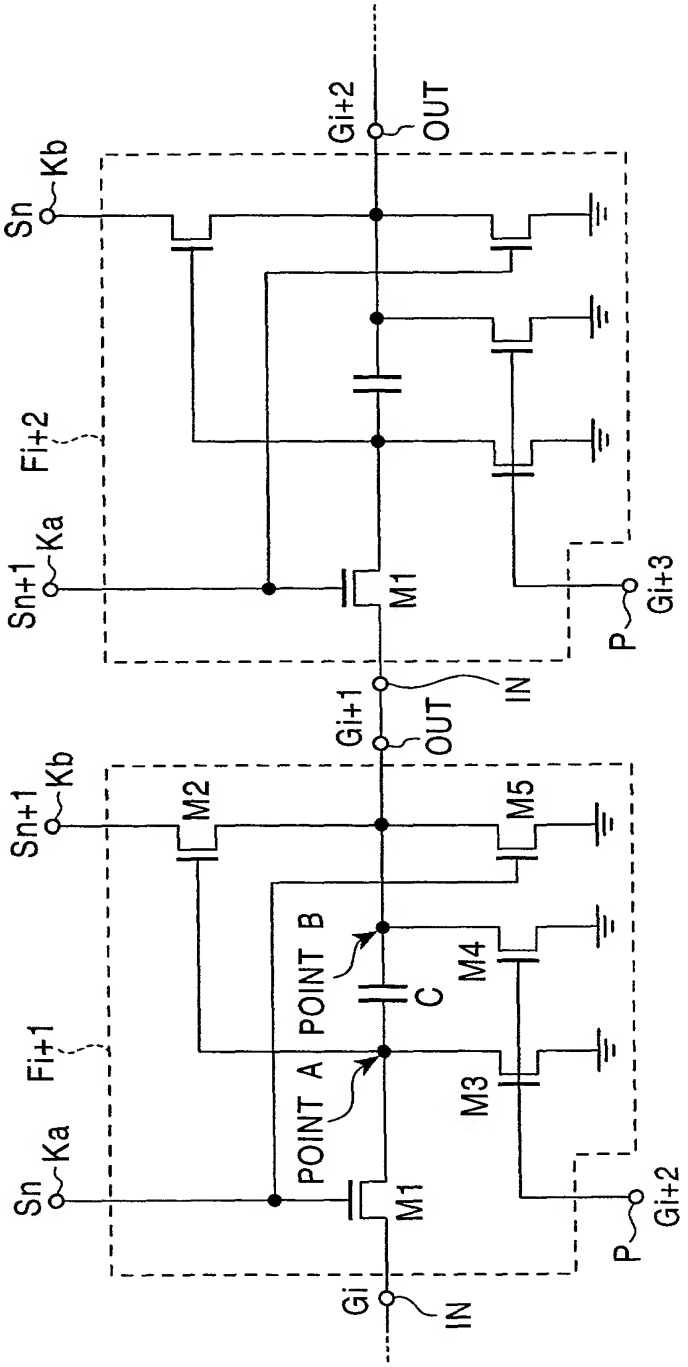

Gi+2
OUT
Sn
Kb
Fi+2
Sn+1
Ka
M1
P
Gi+3
Gi+1
OUT
IN
Sn+1
Kb
M2
M5
POINT B
C
M4
Fi+1
POINT A
M3
Sn
Ka
M1
P
Gi+2
Gi
IN

FIG. 13

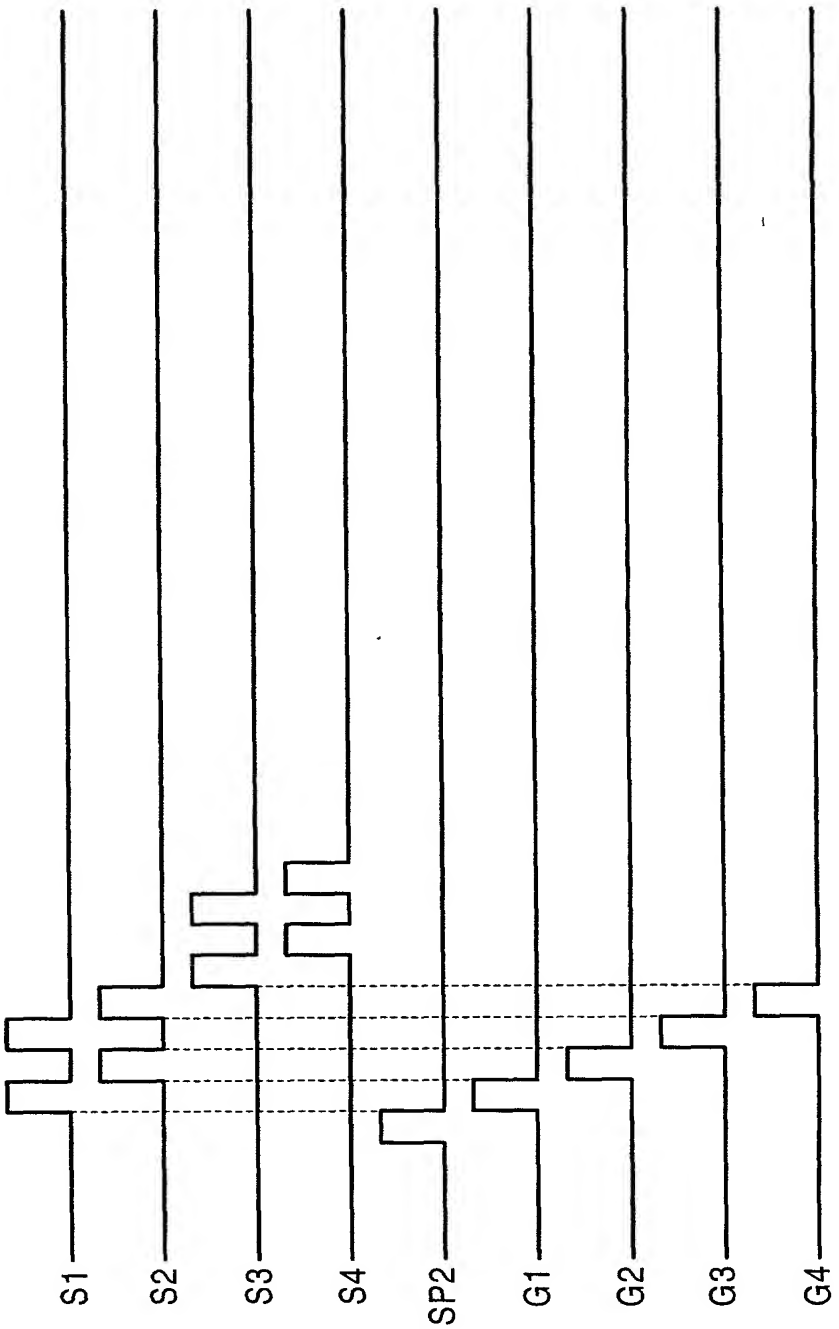


FIG. 14

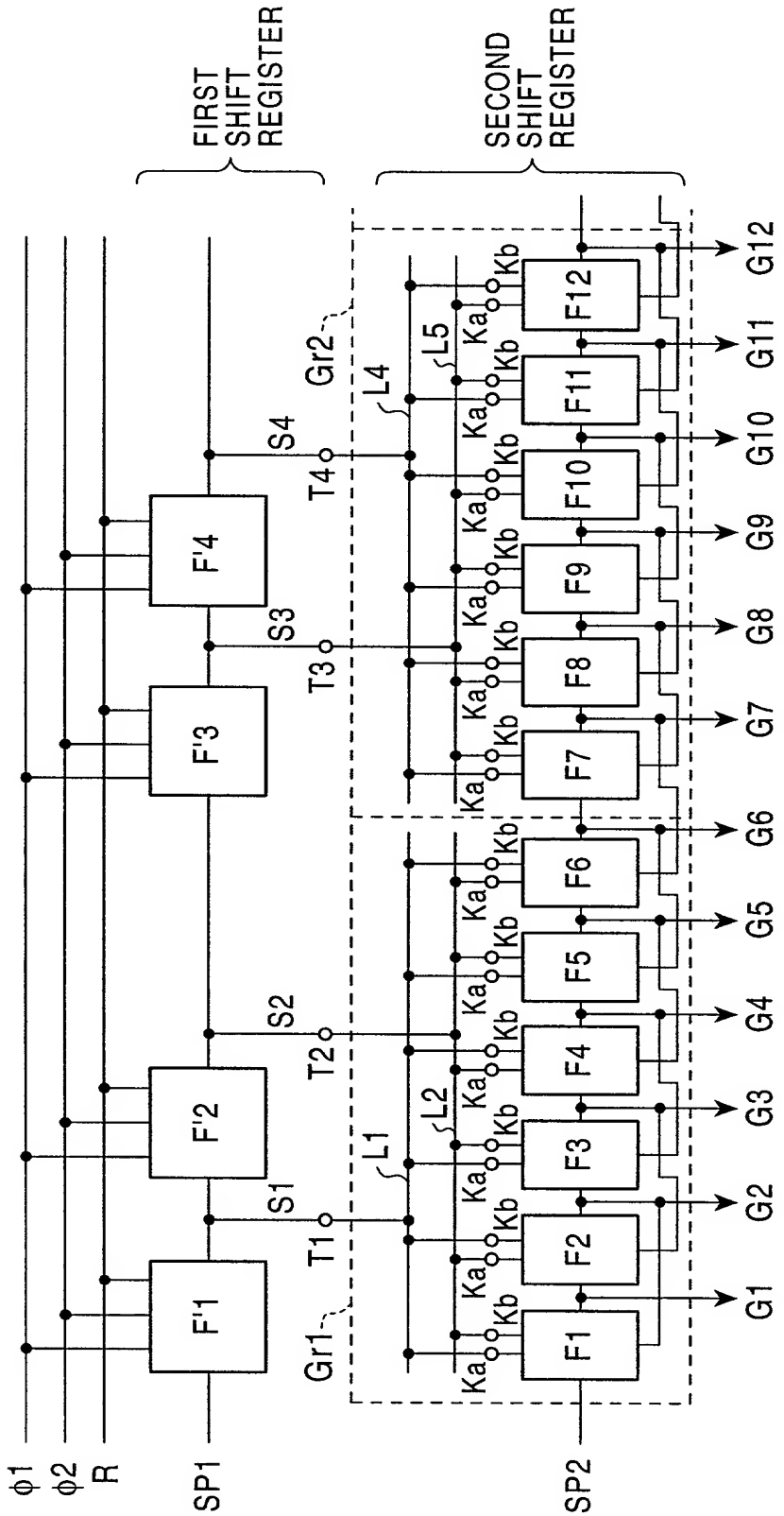
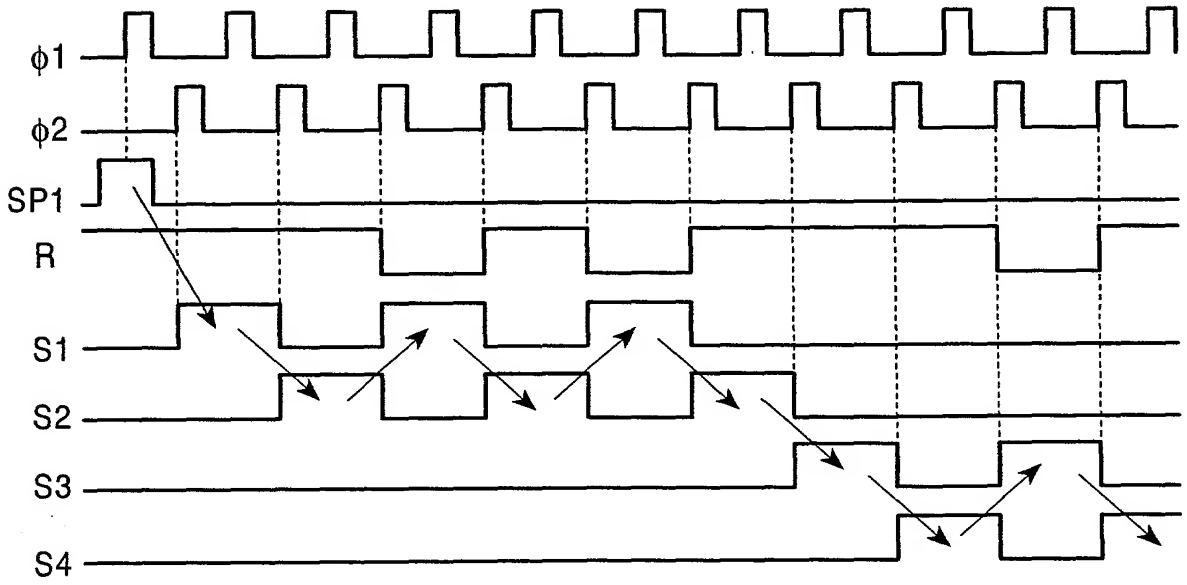

FIRST SHIFT REGISTER
SECOND SHIFT REGISTER
φ1
φ2
R
SP1
SP2
F'1
F'2
F'3
F'4
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
Gr1
Gr2
T1
T2
T3
T4
S1
S2
S3
S4
L1
L2
L4
L5
Ka
Kb
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
G11
G12

FIG. 15



Replacement Sheet

FIG. 16

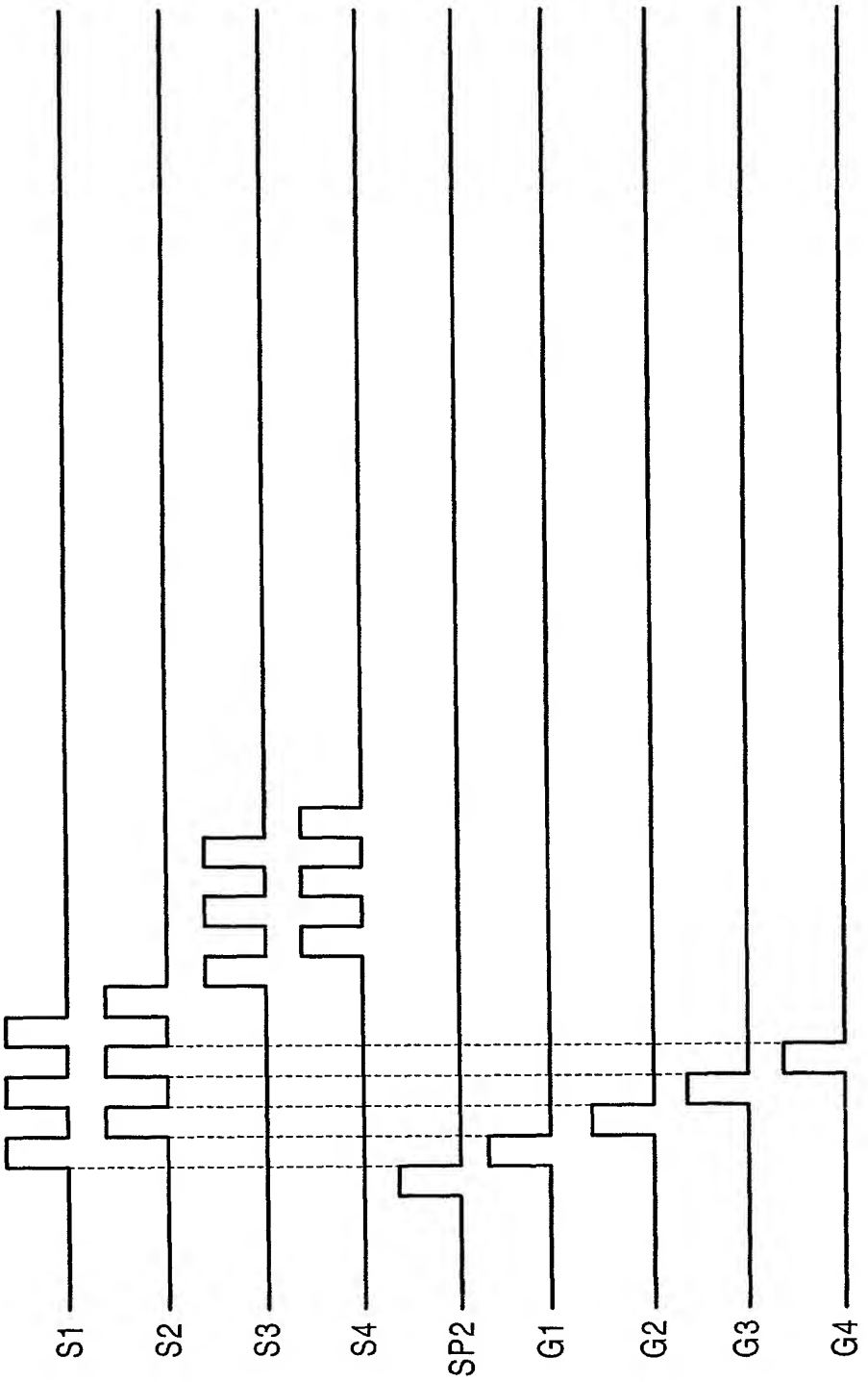


FIG. 17

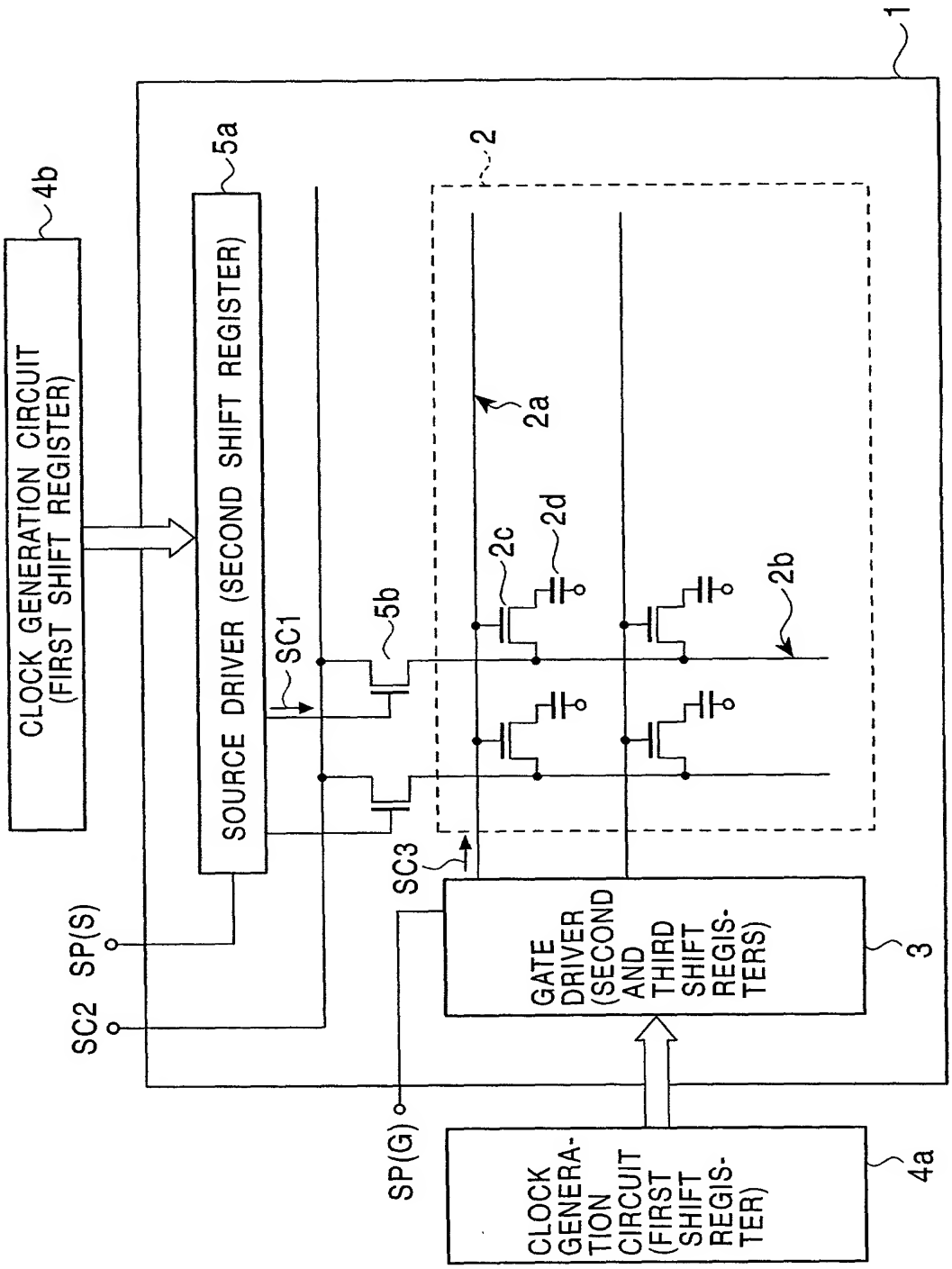

1
2
2a
2b
2c
2d
3
4a
4b
5a
5b
CLOCK GENERATION CIRCUIT (FIRST SHIFT REGISTER)
SOURCE DRIVER (SECOND SHIFT REGISTER)
SC1
SC2
SC3
SP(S)
SP(G)
GATE DRIVER (SECOND AND THIRD SHIFT REGIS-TERS)
CLOCK GENERA-TION CIRCUIT (FIRST SHIFT REGIS-TER)

FIG. 18

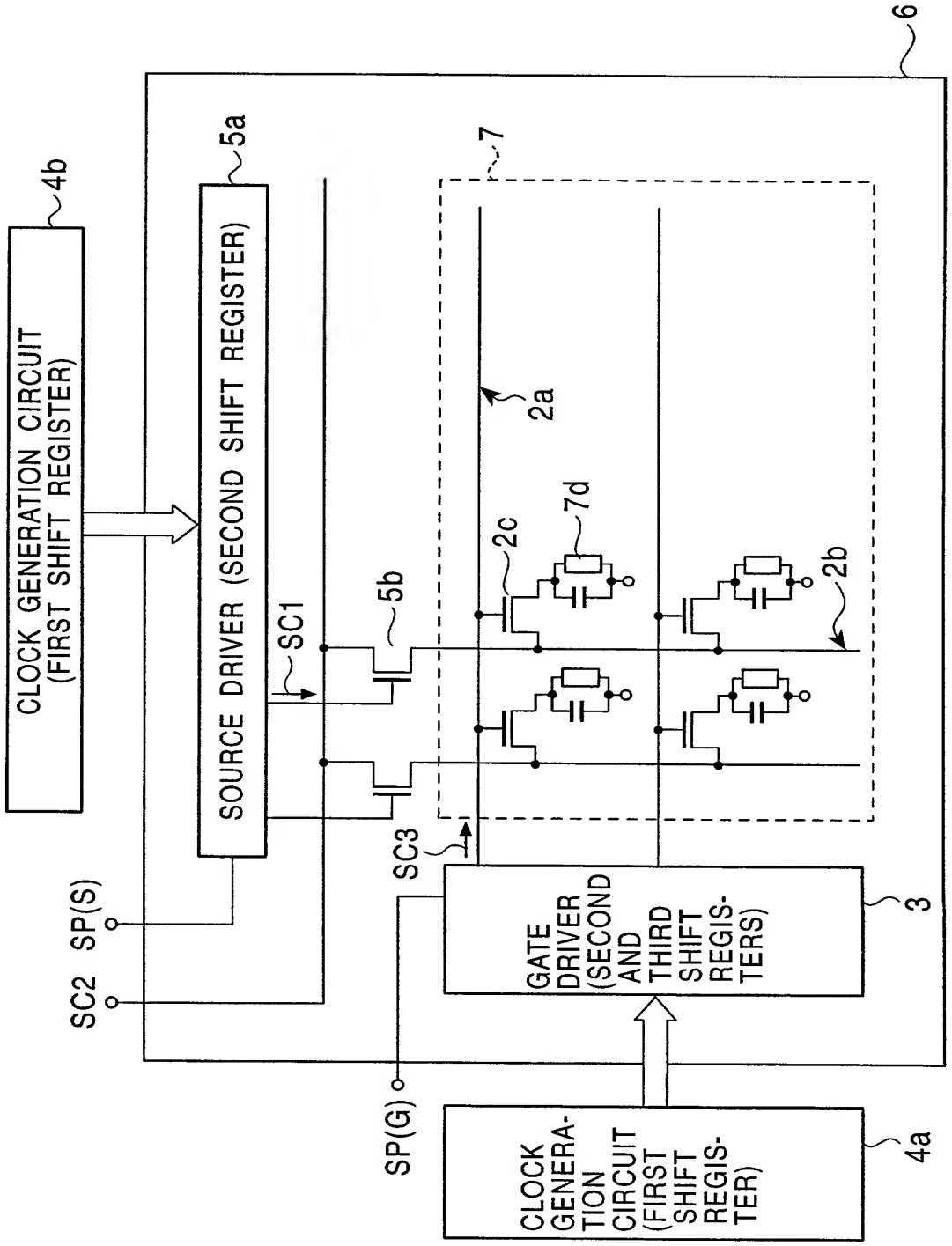
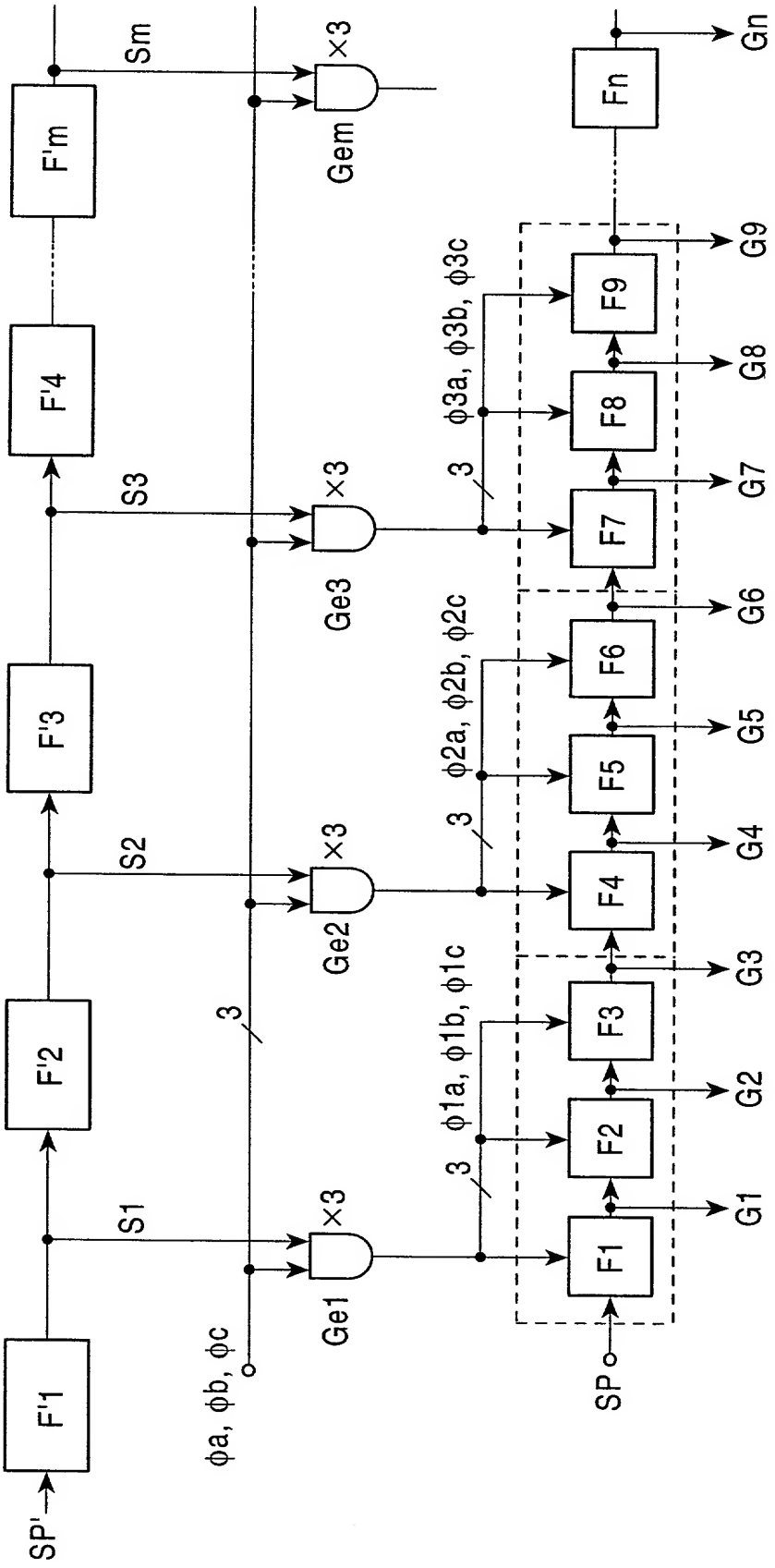

6
4b
CLOCK GENERATION CIRCUIT (FIRST SHIFT REGISTER)
5a
SOURCE DRIVER (SECOND SHIFT REGISTER)
7
2a
2c
7d
2b
5b
SC1
SC3
SC2
SP(S)
SP(G)
GATE DRIVER (SECOND AND THIRD SHIFT REGISTERS)
3
CLOCK GENERATION CIRCUIT (FIRST SHIFT REGISTER)
4a

FIG. 19


SP'
F'1
F'2
F'3
F'4
F'm
Sm
S3
S2
S1
Gem
Ge3
Ge2
Ge1
×3
3
φa, φb, φc
SP
F1
F2
F3
F4
F5
F6
F7
F8
F9
Fn
φ1a, φ1b, φ1c
φ2a, φ2b, φ2c
φ3a, φ3b, φ3c
G1
G2
G3
G4
G5
G6
G7
G8
G9
Gn

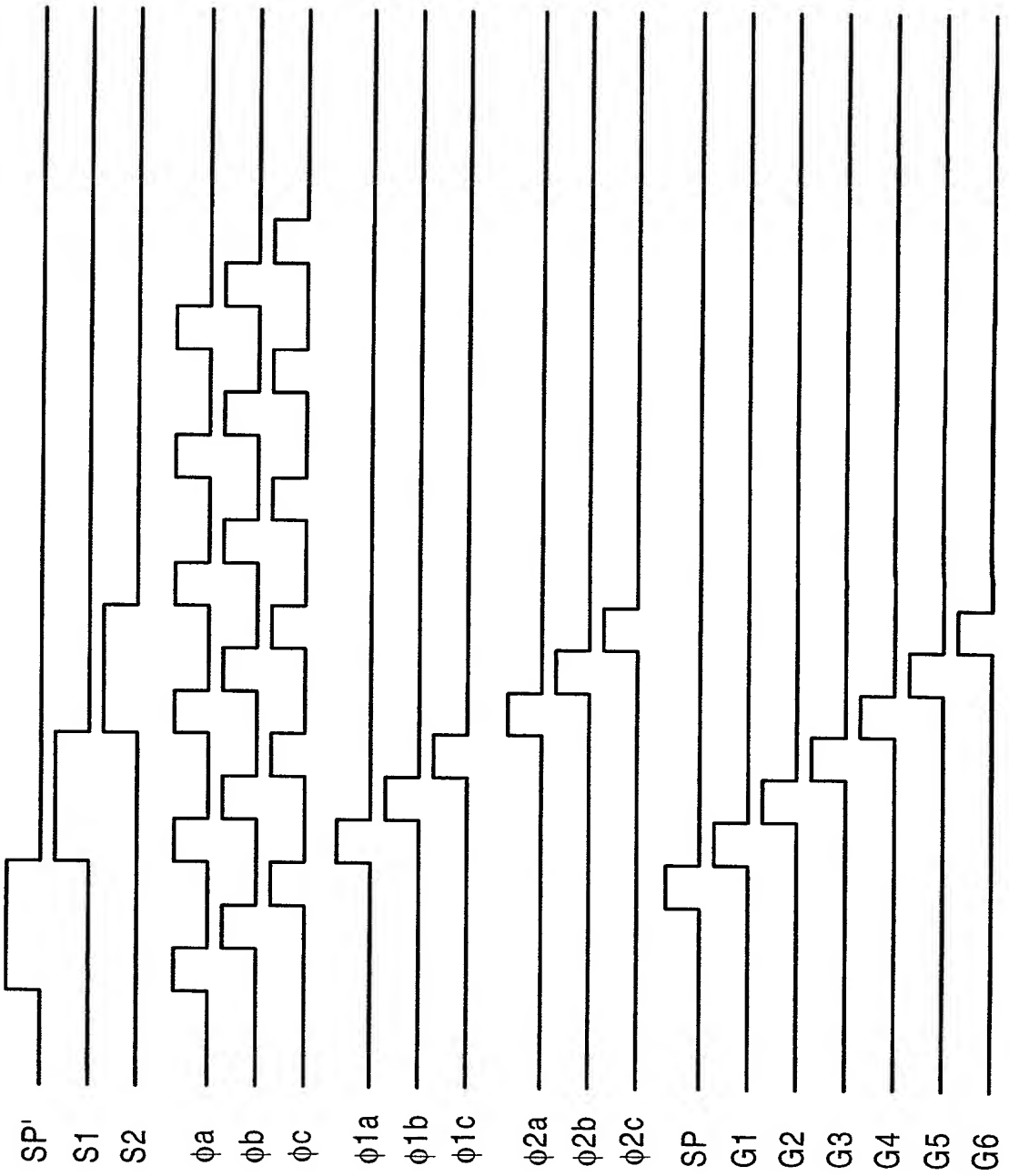



FIG. 20